

EVADC

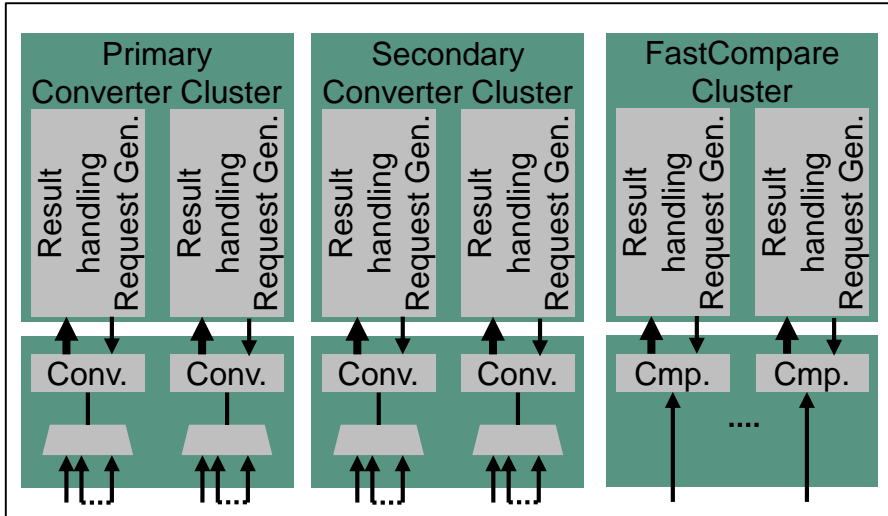
Enhanced Versatile Analog-to-Digital Converter

AURIX™ TC3xx Microcontroller Training
V1.0 2020-09



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Enhanced Versatile Analog-to-Digital Converter



Highlights

- › Up to 12 independent converters with up to 16 analog input channels each
- › Conversion time below 500 ns is possible (below 200 ns for a Fast Compare cluster)
- › Flexible source selection and arbitration
- › Powerful result handling

Key Features

- › Flexible source selection and arbitration
- › Powerful conversion result handling

Customer Benefits

- › Programmable arbitration and conversion sequence
- › Extended conversion sequences
- › Independent result registers with selectable FIR/IIR filters
- › Data rate reduction

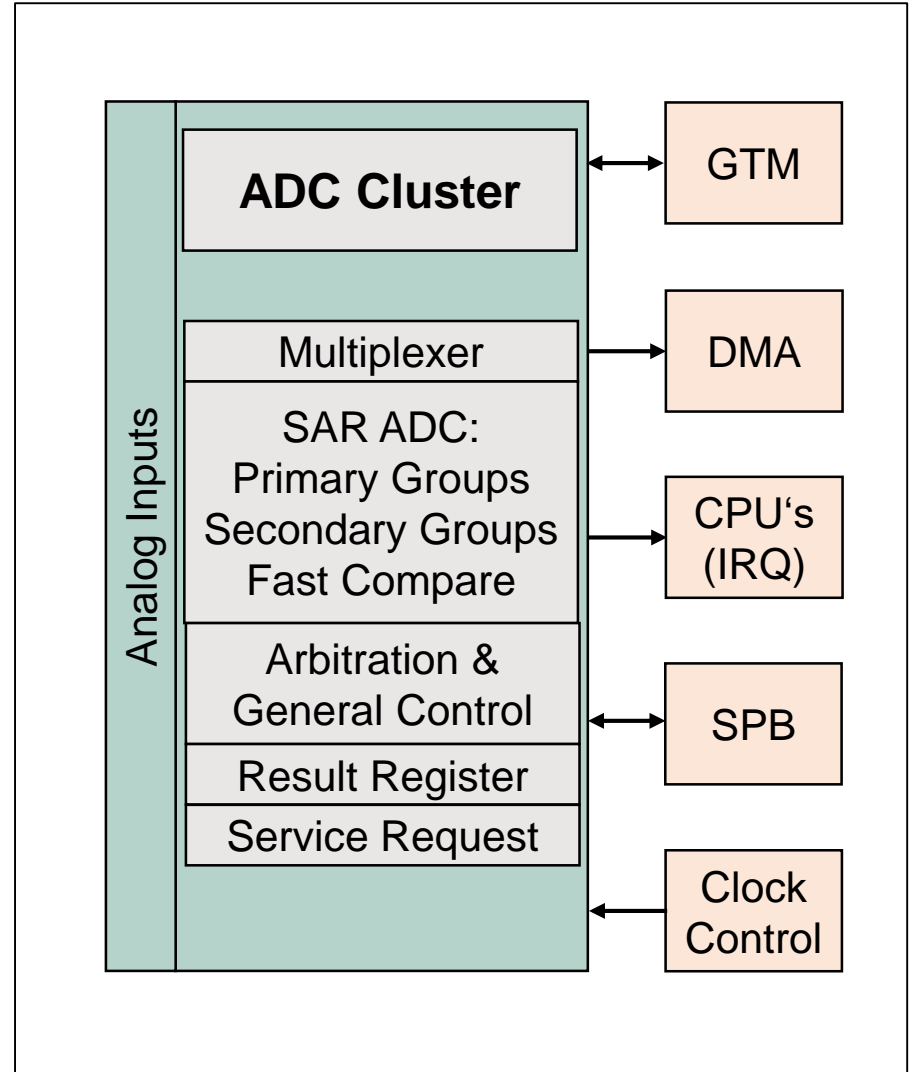
Flexible source selection and arbitration

- › Programmable arbitrary conversion sequence (single or repeated)
- › Request source chaining to generate extended conversion sequences
- › Conversions triggered by software, timer events, or external events
- › Cancel-inject-restart mode for reduced conversion delay on priority channels
- › External analog multiplexer control, including adjusted sample time and scan support
- › Conversion speed and sample time adjustable to adapt to sensors and reference

Powerful conversion result handling

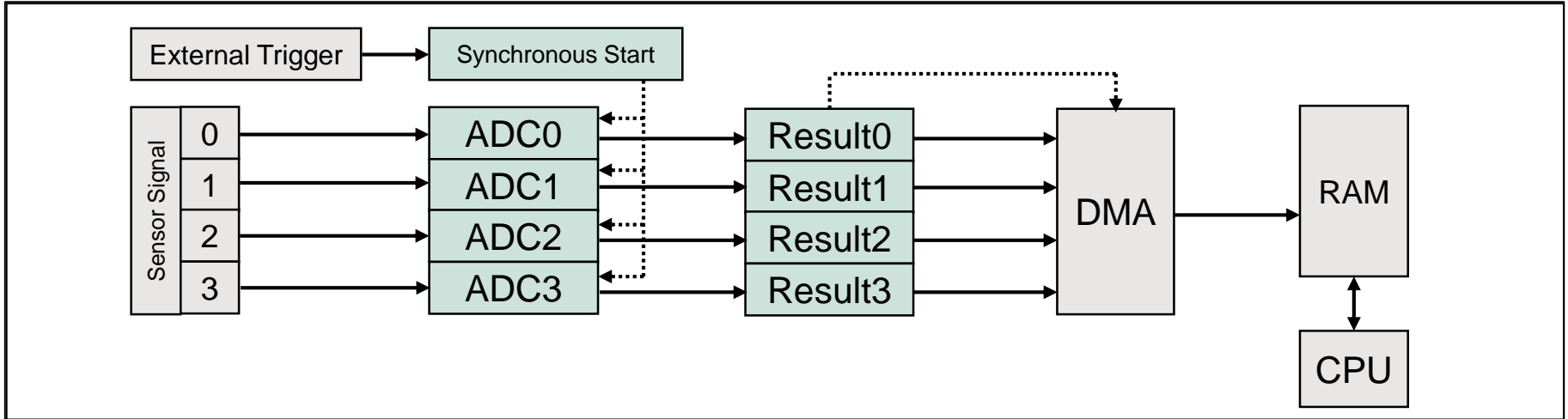
- › FastCompare Cluster compares result register content directly with input signal
- › Storage of conversion results to user-configurable registers
- › Configurable limit checking against programmable border values
- › Data alignment according to result width and endianness
- › Wait-for-Read mode to avoid loss of data
- › Data rate reduction through adding a selectable number of conversion results
- › Result event generation
- › Data reduction or anti-aliasing filtering. FIR/IIR filter with selectable coefficients

- › The analog inputs are connected to a cluster of Analog/Digital Converters which convert analog input values (voltages) to discrete digital values
- › Each converter of the ADC cluster can operate independently of the others
- › The results of each channel can be stored in a dedicated channel-specific result register or in a group-specific result register



Application example

Synchronized conversions



Overview

- > Synchronized Conversions for parallel sampling
- > Result handling via DMA (Direct Memory Access)

Advantages

- > Several independent ADC kernels can be synchronized for simultaneous measurements of analog input channels
- > Synchronization for parallel conversions ensures that the sample phases of the related channels start simultaneously

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