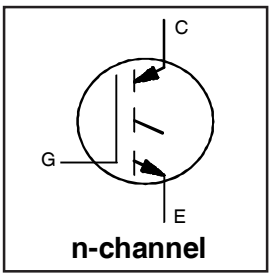
International
IOR Rectifier

PDP TRENCH IGBT

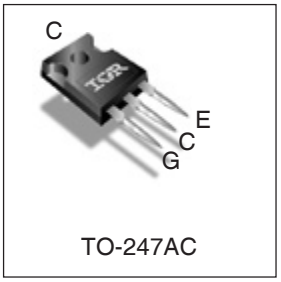
IRG7PC28UPbF

Features
- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
V_{CE} min	600	V
$V_{CE(ON)}$ typ. @ I_C = 40A	1.70	V
I_{RP} max @ T_C= 25°C ①	225	A
T_J max	150	°C



n-channel



TO-247AC

G	C	E
Gate	Collector	Emitter

Description
This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	±30	V
I_C @ T_C = 25°C	Continuous Collector Current, V_{GE} @ 15V	61	A
I_C @ T_C = 100°C	Continuous Collector, V_{GE} @ 15V	33	
I_{RP} @ T_C = 25°C	Repetitive Peak Current ①	225	
P_D @T_C = 25°C	Power Dissipation	160	W
P_D @T_C = 100°C	Power Dissipation	64	
	Linear Derating Factor	1.3	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	0.78	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink ②	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_{CE} = 1.0mA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage③	15	—	—	V	V_{GE} = 0V, I_{CE} = 1.0A
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.57	—	V/°C	Reference to 25°C, I_{CE} = 1.0mA
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.25	—	V	V_{GE} = 15V, I_{CE} = 12A ③
		—	1.42	—		V_{GE} = 15V, I_{CE} = 24A ③
			1.70	1.95		V_{GE} = 15V, I_{CE} = 40A ③
		—	1.96	—		V_{GE} = 15V, I_{CE} = 70A ③
		—	2.97	—		V_{GE} = 15V, I_{CE} = 160A ③
		—	1.75	—		V_{GE} = 15V, I_{CE} = 40A, T_J = 150°C ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	V_{CE} = V_{GE}, I_{CE} = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I_{CES}	Collector-to-Emitter Leakage Current	—	0.5	20	µA	V_{CE} = 600V, V_{GE} = 0V
		—	30	—		V_{CE} = 600V, V_{GE} = 0V, T_J = 100°C
		—	90			V_{CE} = 600V, V_{GE} = 0V, T_J = 125°C
		—	305	—		V_{CE} = 600V, V_{GE} = 0V, T_J = 150°C
I_{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	V_{GE} = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V_{GE} = -30V
g_{fe}	Forward Transconductance	—	55	—	S	V_{CE} = 25V, I_{CE} = 40A
Q_g	Total Gate Charge	—	70	—	nC	V_{CE} = 400V, I_C = 40A, V_{GE} = 15V③
Q_{gc}	Gate-to-Collector Charge	—	25	—		
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	I_C = 40A, V_{CC} = 400V
t_r	Rise time	—	35	—		R_G = 22Ω, L=100µH
$t_{d(off)}$	Turn-Off delay time	—	260	—		T_J = 25°C
t_f	Fall time	—	145	—		
$t_{d(on)}$	Turn-On delay time	—	25	—	ns	I_C = 40A, V_{CC} = 400V
t_r	Rise time	—	40	—		R_G = 22Ω, L=100µH
$t_{d(off)}$	Turn-Off delay time	—	280	—		T_J = 150°C
t_f	Fall time	—	320	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	V_{CC} = 240V, V_{GE} = 15V, R_G= 5.1Ω
E_{PULSE}	Energy per Pulse	—	770	—	µJ	L = 220nH, C= 0.40µF, V_{GE} = 15V V_{CC} = 240V, R_G= 5.1Ω, T_J = 25°C
		—	930	—		L = 220nH, C= 0.40µF, V_{GE} = 15V V_{CC} = 240V, R_G= 5.1Ω, T_J = 100°C
ESD	Human Body Model	Class H1C (2000V) (Per JEDEC standard JESD22-A114)				
	Machine Model	Class M4 (425V) (Per EIA/JEDEC standard EIA/JESD22-A115)				
C_{ies}	Input Capacitance	—	1880	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	75	—		V_{CE} = 30V
C_{res}	Reverse Transfer Capacitance	—	45	—		f = 1.0MHz
L_C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

① Half sine wave with duty cycle <= 0.02, ton=1.0µsec.

② R_θ is measured at T_J of approximately 90°C.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

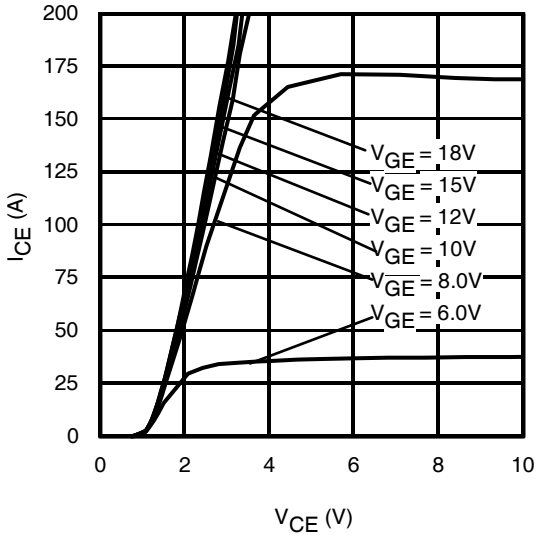


Fig 1. Typical Output Characteristics @ 25°C

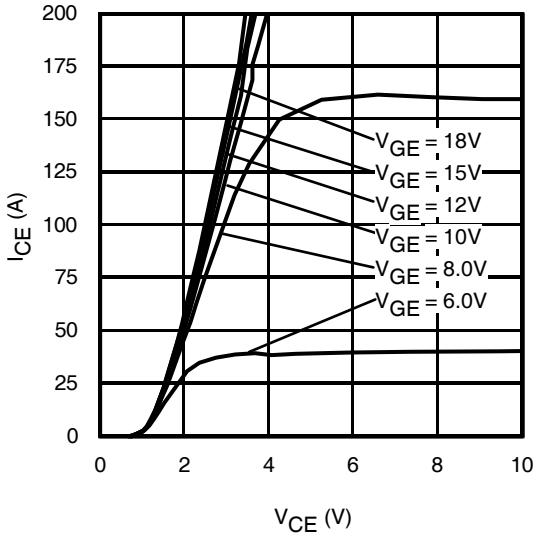


Fig 2. Typical Output Characteristics @ 75°C

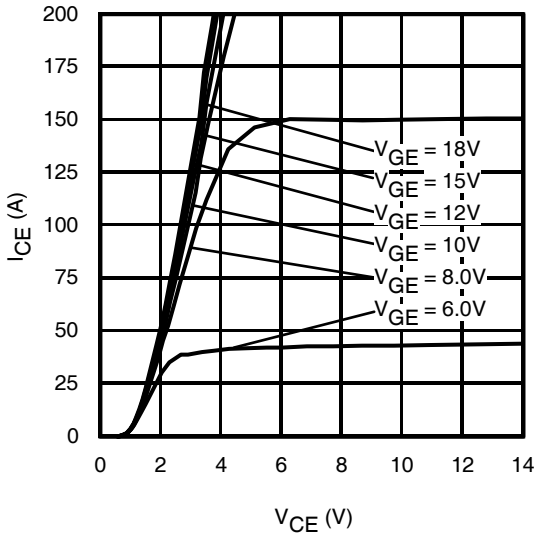


Fig 3. Typical Output Characteristics @ 125°C

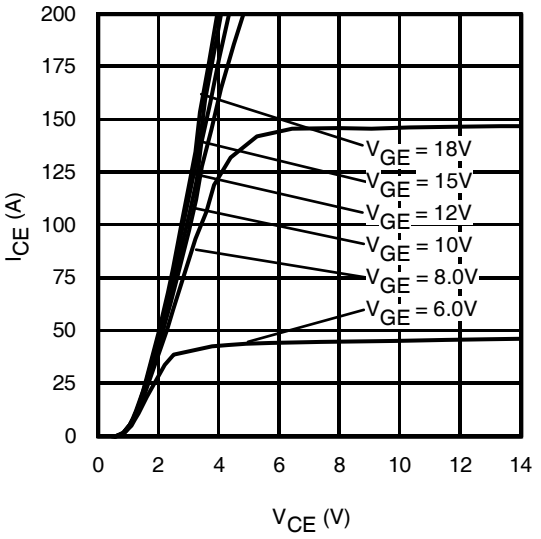


Fig 4. Typical Output Characteristics @ 150°C

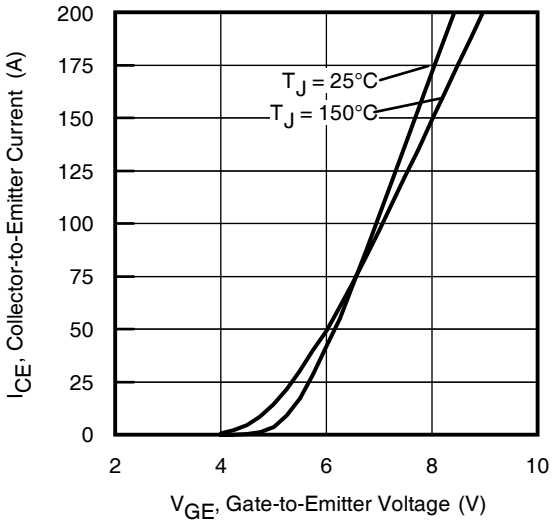


Fig 5. Typical Transfer Characteristics

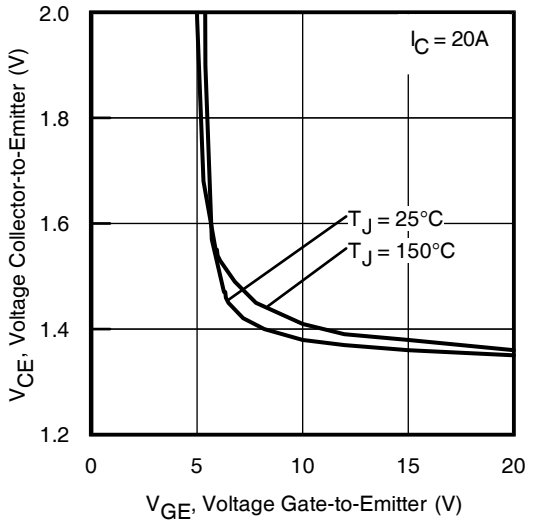


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

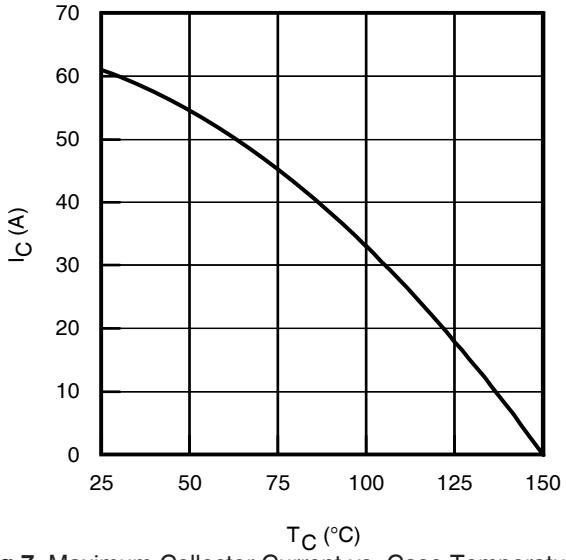


Fig 7. Maximum Collector Current vs. Case Temperature

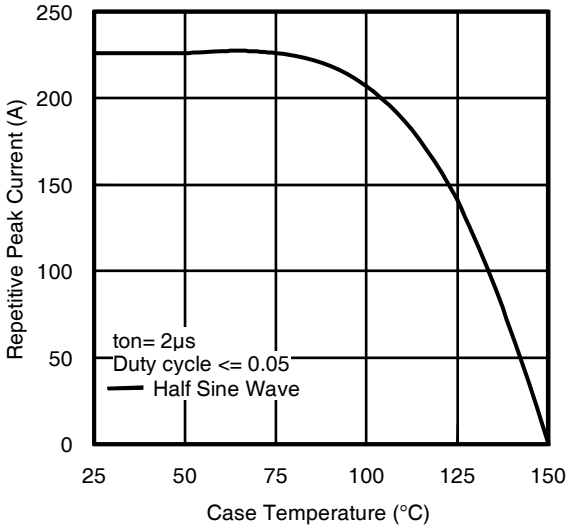


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

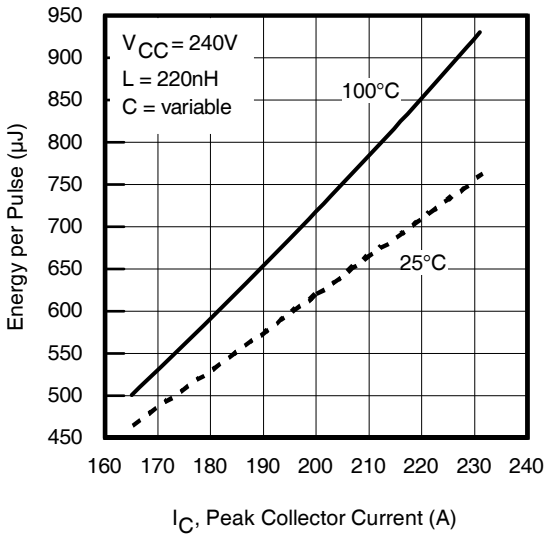


Fig 9. Typical E_{PULSE} vs. Collector Current

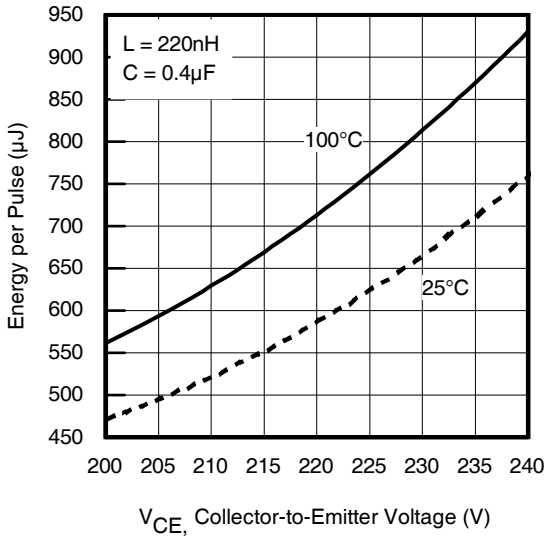


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

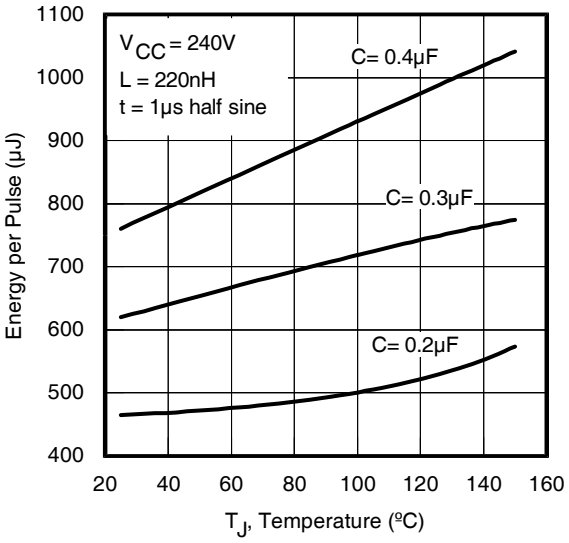


Fig 11. E_{PULSE} vs. Temperature

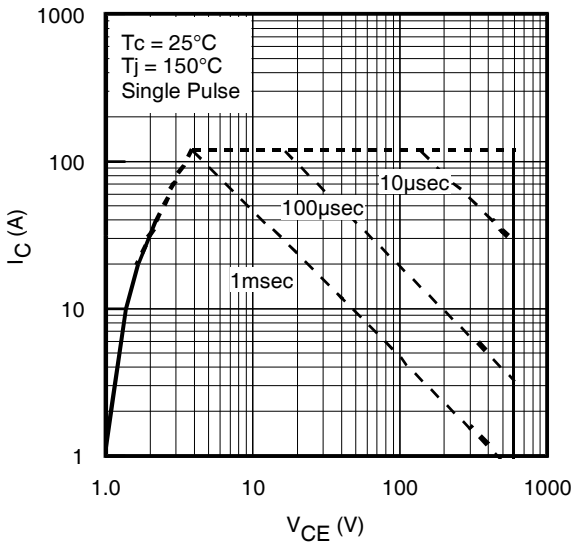


Fig 12. Forrward Bias Safe Operating Area

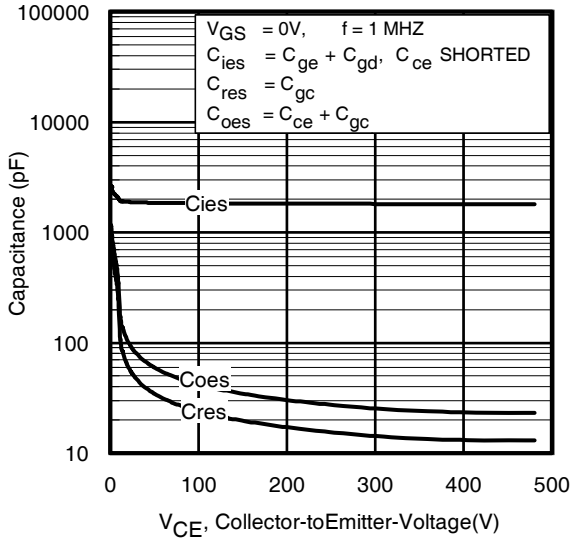


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

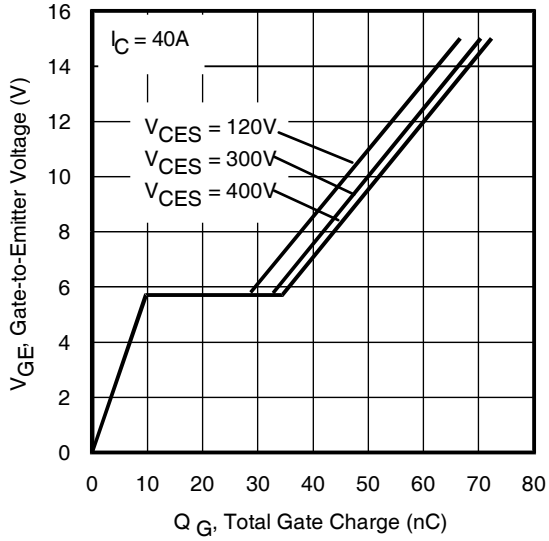


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

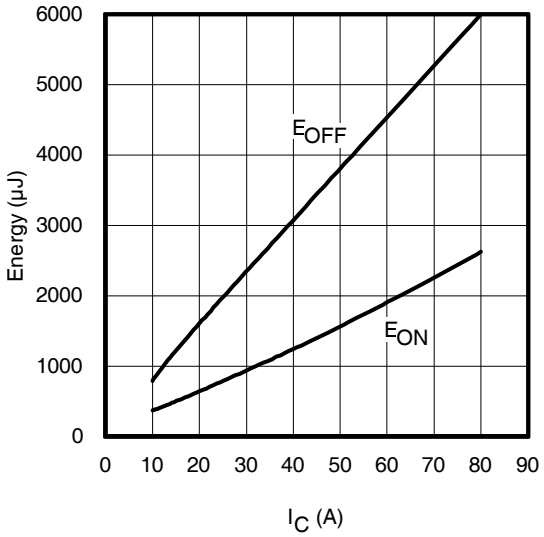


Fig. 15 - Typ. Energy Loss vs. I_C
T_J = 150°C; L = 250µH; V_{CE} = 400V, R_G = 22Ω; V_{GE} = 15V

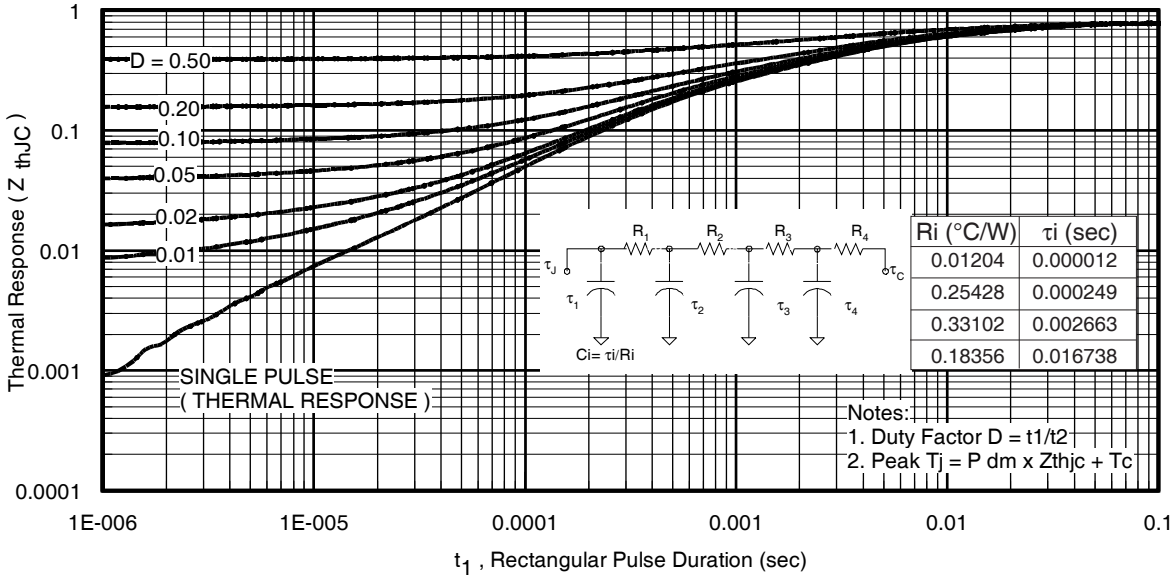


Fig 16. Maximum Effective Transient Thermal Impedance, Junction-to-Case

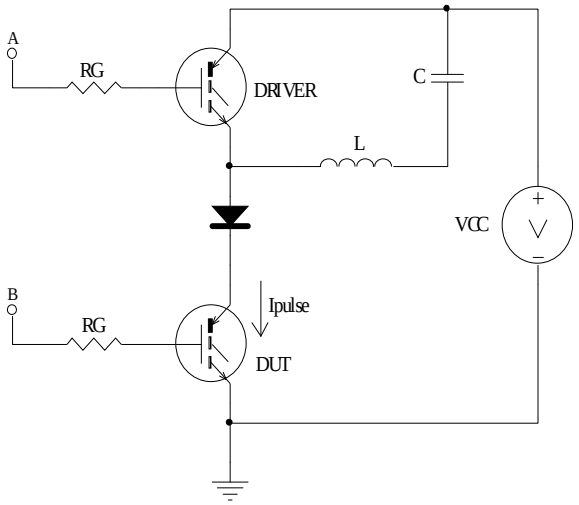


Fig 16a. t_{st} and E_{PULSE} Test Circuit

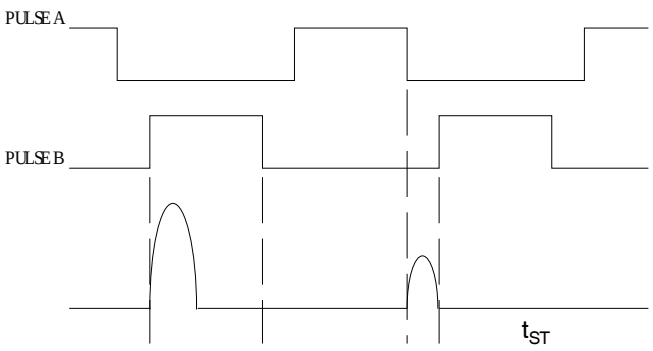


Fig 16b. t_{st} Test Waveforms

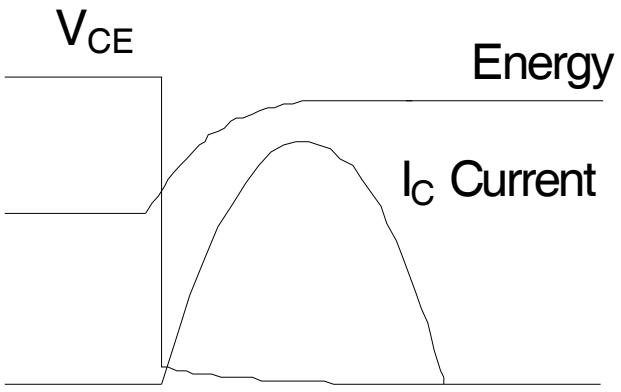


Fig 16c. E_{PULSE} Test Waveforms

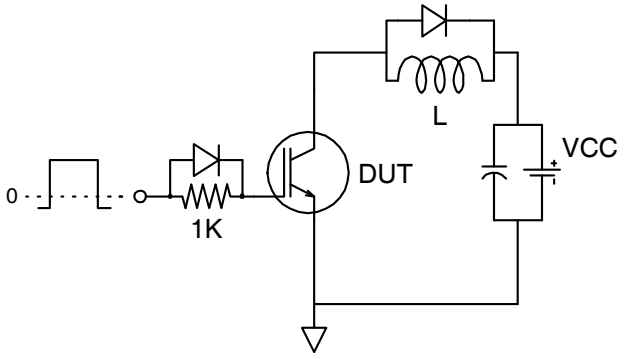
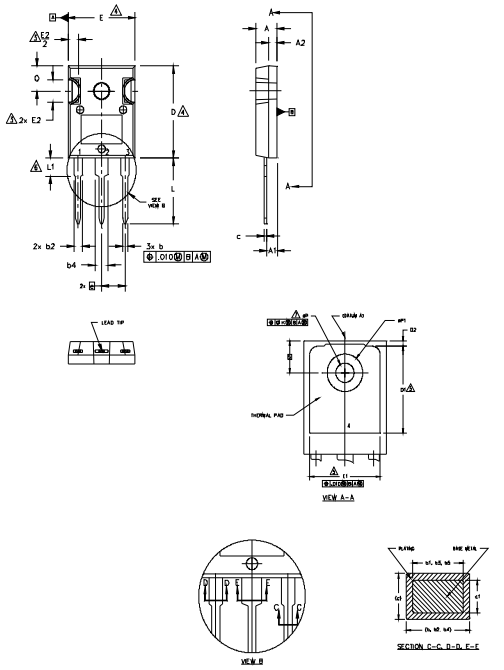


Fig. 17 - Gate Charge Circuit (turn-off)

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

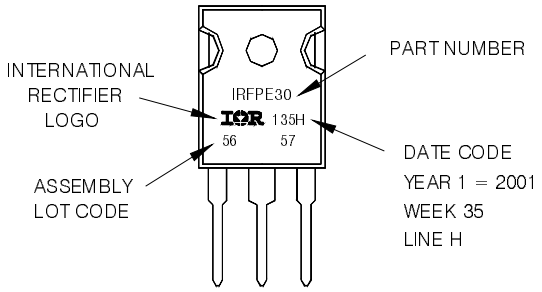
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

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Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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